**Part 5 - Report**

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**What did you learn from this project?**

The project provided great insight into the design challenges and considerations needed for the design of a processor. Our experiences with the RISC architecture we implemented have given us a solid foundation for the understanding of the design of a datapath. Our particular datapath was a single cycle design with separate instruction and data memories. We found that a single physical memory was impossible to implement in a single cycle as the same bus would need to be asynchronously used for both read and write at the same time. We also developed a control logic unit which needed to consider certain bus contentions to avoid data corruption and incorrect output. The project also provided some valuable lessons in teamwork and time-management that apply to all projects.

**What would you do differently next time?**

More research would have been a great benefit to us before we actually began the design. Some more thorough development of the datapath and instruction set early on could have saved a lot of debugging time later. We had to retrofit our instruction set in order to allow for immediate arguments without using new opcodes, research time could have helped limit the time needed in the development of the final instruction set. The reason we learned so much about the need for time management was that we had a tendency to do most of the work in long sessions, rather than in smaller bits of time spread out over the semester.

**What is your advice to someone who is going to work on a similar project?**

Start early and do plenty of research prior to starting the design. This will really pay off as a savings in time. Computer simulations that work do not indicate a processor that works in the hardware (FPGA). Go to the lab early and try to get your design verified on hardware with plenty of time, there will be inevitable problems with the hardware that did not exist in theory.